IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application of

Applicants	: Jigish D. Trivedi
Serial No.	: 08/915,658
Filed	: August 21, 1997
Title	: LOW RESISTANCE METAL SILICIDE LOCAL INTERCONNECTS AND METHOD OF MAKING
Docket No.	: MIO 0024 PA
Examiner	: Ginette Peralta
Art Unit	: 2814

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BRIEF ON APPEAL

This is an appeal from the Office Action mailed April 4, 2005, finally rejecting claims 31-49. A Notice of Appeal was timely filed on July 5, 2005. Our check in the amount of $500.00 accompanies this Brief. 37 CFR §1.17(c).

Real Party in Interest

The real party in interest is the assignee of this patent application, Micron Technology, Inc., by assignment from the named inventor recorded in the files of the U.S. Patent and Trademark Office at Reel 8682, Frame 0140.

Related Appeals and Interferences

Applicant previously appealed to the Board of Patent Appeals and Interferences on January 2, 2001 under Appeal No. 2002-0043. A copy of the decision rendered in that appeal may be found in the Related Proceedings Appendix attached to this Brief.

Status of Claims

Claims 31-49 stand rejected in this application and are before the Board for consideration on appeal. A copy of the appealed claims is found in the Claims Appendix attached to this Brief.

Status of Amendments

All of the amendments previously filed in this application have been entered with the exception of an Amendment After Final Rejection filed on May 20, 2005. In an Advisory Action mailed June 29, 2005, the Examiner indicated that the amendment would be entered upon the filing of an appeal. Accordingly, the claims in the Claims Appendix reflect entry of that amendment.

Summary of Claimed Subject Matter

The present invention is directed to a low resistance local interconnect which is formed by providing a metal layer over a semiconductor layer, forming a metal silicide layer over the layer of metal, annealing the layers to form a composite structure, and removing unreacted metal from the metal layer. Referring to Figs. 3-7 and the specification at pages 12-13, a layer of a first metal silicide 34 (preferably tungsten-silicide,WSi_x) is formed over a metal layer 32 (such as Ti), and a layer of photoresist 36 is formed over the metal silicide layer 34, and is patterned and etched to form a structure 34A which defines the boundaries of the local interconnect. The patterned structure 34A is then reacted with the underlying metal layer 32 by annealing to form a composite structure 37. The composite structure 37 includes the first metal silicide, and a second metal silicide (such as titanium-silicide, $TiSi_2$) formed by the reaction of silicon from metal silicide 34 with underlying metal 32. The composite structure also includes an intermetallic compound (such as TiW) which comprises metal from the first metal silicide 34 (such as W) and metal from the underlying metal layer 32 Ti (which is converted to second metal silicide $TiSi_2$). Thus, the intermetallic compound comprises a metal from the first metal silicide (such as W) and a metal from a second metal silicide (such as Ti). The intermetallic compound reduces the resistance of the local interconnect.

In one embodiment of the invention described in the specification at pages 9 and 10, the local interconnect may be used to connect a first active semiconductor region to a second

activate semiconductor region on a substrate assembly 10. For example, as shown in Figs. 3-7, the local interconnect may be used to connect a gate (G) of one MOSFET to the drain (D) or source (S) of another MOSFET. As shown, the first and second active semiconductor regions are separated by an insulating region (field oxide 16).

As shown in Fig. 8 and as described in the specification at page 14, one or more interconnects 37 may also be used to connect various structures in an integrated circuit 40, such as the gates of two or more transistors 14, and respective sources to respective drains.

As shown in Figs. 9 and 10 and as described in the specification at pages 14 (lines 22-29) and 15 (lines 1-9), one or more local interconnects 37 may be used in a memory array such as a static random access memory (SRAM) or a dynamic random access memory (DRAM). The memory array includes a plurality of memory cells 46 arranged in rows and columns and formed on a substrate having at least one semiconductor layer, with each of the plurality of memory cells comprising at least one field effect transistor 14. The local interconnect connects at least one of a source, drain or gate of the field effect transistor in one of the plurality of memory cells to an active area within one memory cell or to one of a source, drain, or gate of the field effect transistor in another one of the plurality of memory cells.

Grounds of Rejection to be Reviewed on Appeal

The grounds of rejection for review on appeal are:

1) Claims 31-35, 37, 41-45 and 48-49 stand rejected under 35 U.S.C. 102(b) as being anticipated by Chung et al. (U.S. 5,094,981).

2) Claims 36, 38-40 and 46-47 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al. in view of Okamoto (U.S. 4,910,578).

Grouping of Claims

The Examiner has made two grounds of rejection, rejecting claims 31-35, 37, 41-45 and 48-49 under 35 U.S.C. 102(b) as being anticipated by Chung et al. (U.S. 5,094,981); and rejecting claims 36, 38-40 and 46-47 under 35 U.S.C. 103(a) as being unpatentable over Chung et al. in view of Okamoto (U.S. 4,910,578). The application contains five independent claims, namely, claim 31, 35, 37, 38, and 41. Applicant submits that the claims do not stand or fall together. The patentability of each independent claim will be separately argued.

Argument

Rejection under 35 U.S.C. 102(b) in view of Chung et al. U.S. Patent No. 5,094,981

Claim 31

Claim 31 is directed to a local interconnect comprising a composite structure comprising a first metal silicide, a second metal silicide, and an intermetallic compound reducing the resistance of the local interconnect, where the intermetallic compound comprises metal from the first metal silicide and metal from the second metal silicide, and where the intermetallic compound contains no non-metallic materials.

Chung et al., U.S. Patent No. 5,094,981, is directed to a method for providing interconnections for a semiconductor having low contact resistance in which a contact layer of titanium 34 is deposited onto a semiconductor device followed by a barrier material 36 comprised of titanium-tungsten or tungsten. The structure is annealed, followed by deposition of an interconnect layer comprising aluminum. The structure is then etched such that remaining portions of the aluminum form items 40A-40C and a composite interconnect layer is formed which contains the aluminum portions 40A-40C along with remaining portions of layers 36 and 34.

In the final rejection mailed April 4, 2005, the Examiner asserted that Chung et al. teach a composite structure comprising a first metal silicide (38A, 38B), a second metal silicide (40A, 40B), and an intermetallic compound (36A, 36B). The Examiner further asserted that the

"intermetallic compound" of Chung comprises a metal from the first metal silicide and a metal from the second metal silicide, where "the first metal silicide is titanium silicide" and "the second metal silicide is tungsten silicide."

Applicants previously pointed out that the composite structure of Chung et al. does not include metal silicide layer 38, but rather includes only remaining portions of layer 34 (titanium contact layer) and layer 36 (titanium-tungsten or tungsten barrier layer), and layer 40 (interconnect layer comprising aluminum or aluminum alloy). See the last sentence of Chung's abstract and col. 5, lines 64-66.

In the Advisory Action mailed June 29, 2005, the Examiner maintained that Chang's composite structure includes layer 38, reasoning that "layer 38 is formed by treating layer 34." Applicant disagrees with the Examiner's reasoning. There is no teaching or suggestion in Chung which indicates that any portion of layer 38 is present in layers 34 or 36, which layers become part of the composite structure upon etching. While Chung teaches that the layers 38A-38C are formed along the interfaces of the N-channel FET, P-channel FET, and source/drain zone, such layers are formed **below** layers 34 and 36. Chung clearly teaches that, after etching, the composite structure comprises portions 40A-40C, which comprise remaining portions of deposited aluminum and the remaining portions of layers 36 and 34 (after etching). See col. 5, lines 63-66 and claim 1. The Examiner cannot ignore Chung's teachings and define the composite as including the layers she chooses.

Further, even if Chung's composite included titanium-silicide layers 38, there is no teaching or suggestion in Chung et al. that their intermetallic layer 36 is formed from the metal in layer 38 and the metal in layer 40. Rather, Chung et al. clearly teach that layer 36 is formed by sputter depositing titanium-tungsten onto layer 34, and that layer 38 is formed as a result of annealing the structure including layers 34 and 36. In order for there to be anticipation of applicant's claimed composite, Chung's intermetallic layer 36 would have to be formed from respective metals in the metal silicide layers in Chung, which is clearly not the case here.

Accordingly, Chung et al. teach a composite structure comprised of various metals, i.e., aluminum layer 40, titanium-tungsten or tungsten layer 36, and titanium layer 34, but do not teach a structure including an intermetallic layer which comprises a metal from the first metal silicide and the second metal silicide as claimed. Chang's intermetallic layer 36 is clearly not

formed as taught in the present invention, i.e., from annealing underlying layers Ti and WSi as taught in the present invention, but rather is deposited in the form of an intermetallic layer. Such differences in Chung's process result in compositional differences in the final structure. Claim 31 is clearly patentable over Chang et al.

The Examiner has further maintained that applicant's claims are anticipated if one chooses tungsten silicide from Chung's teaching of alternative materials which may be substituted for aluminum, i.e., copper, tungsten, titanium-tungsten, titanium silicide, and tungsten silicide. However, as applicant previously pointed out, one would have to specifically choose tungsten silicide from Chung's listing of alternative materials, and the act of choosing would negate anticipation. Even if one were to substitute tungsten-silicide for aluminum, an intermetallic layer would not be formed which comprises the metal from the first metal silicide and the metal from the second metal silicide. As pointed out above, Chung's intermetallic (TiW) compound 36 is not formed from annealing any underlying layers as taught in the present invention, but rather is deposited in the form of an intermetallic compound.

Claims 32-34, which depend directly or indirectly from claim 31, are patentable for the same reasons that claim 31 is patentable.

Claim 35

Claim 35 is directed to a local interconnect for connecting a first active semiconductor region to a second active semiconductor region on a substrate assembly, where the first and second active semiconductor regions are separated by an insulating region. The local interconnect comprises a composite structure comprising a first refractory metal silicide, a second refractory metal silicide, and an intermetallic compound comprising a refractory metal from the first refractory metal silicide and the second refractory metal silicide, where the refractory metal from the first refractory metal is different from the refractory metal from the second refractory metal silicide.

With regard to claim 35, the Examiner has taken the position that the local interconnect of Chung et al. meets the claims, asserting that Chung et al. teach a composite structure comprising a first refractory metal silicide (38A, 38B), a second refractory metal silicide (40A, 40B), and an intermetallic compound (36A, 36B), where the intermetallic compound comprises

refractory metal from the first refractory metal silicide and refractory metal from the second refractory metal silicide, and where the refractory metal from the first refractory metal is different from the refractory metal from the second refractory metal.

As applicants pointed out above with regard to claim 31, layers 38A, 38B are not part of Chung's composite structure. Even if such layers were considered to be part of Chung's composite, there is no teaching or suggestion in Chung that intermetallic layers 36 contain a metal from layer 38 and a metal from layer 40. Furthermore, in order to meet claim 35, one would have to specifically choose tungsten silicide as a substitute for aluminum. The act of choosing negates anticipation. There is no motivation in Chung for one to make such a substitution. And, even if one were to use tungsten silicide as layer 40, there is no teaching or suggestion in Chung et al. that layers 36 would contain a (different) metal from each of layers 38 and 40. As pointed out above, Chung teaches that layer 36 is formed by depositing titanium-tungsten onto layer 34. Claim 35 is clearly patentable over Chang et al.

Claim 42, which depends from claim 35, is patentable for the same reasons as claim 35.

Claim 37

Claim 37 is directed to a semiconductor device comprising a substrate assembly having at least one semiconductor layer; at least one field effect transistor formed in the semiconductor layer having a source, a drain, and a gate; and a local interconnect for connecting at least one of the source, drain and gate to another activate area within the substrate assembly. The local interconnect comprises a composite structure comprising a first refractory metal silicide, a second refractory metal silicide, and an intermetallic compound comprising refractory metal from the first refractory metal silicide and refractory metal from the second refractory metal silicide.

With regard to claim 37, the Examiner has taken the position that Chung et al. discloses a semiconductor device comprising a substrate having at least one semiconductor layer (10), at least one field effect transistor (22) having a source (18), a drain (18), and a gate (22), and a local interconnect that comprises a composite structure comprising a first refractory metal silicide (38A, 38B), a second refractory metal silicide (40A, 40B), and an intermetallic compound (36A, 36B). As pointed out above, Chung does not teach an intermetallic compound which comprises

a refractory metal from the first refractory metal silicide and a metal from the second refractory metal silicide as claimed. Rather, Chung teaches an intermetallic compound which is sputter deposited as titanium-tungsten. Layer 36 of Chung et al. does not contain metal from the first refractory metal silicide and a metal from the second refractory metal silicide. Claim 37 is patentable for the same reasons discussed above with regard to claims 31 and 35. Claim 41 is also believed to be patentable for the same reasons discussed above with regard to claims 31, 35, and 37.

Claims 44 and 45, which depend directly or indirectly from claim 37, are patentable for the same reasons that claim 37 is patentable.

Claims 32-34, 42-49

The Examiner asserts that the "first metal silicide" (38) of Chung comprises titanium silicide and that the "second metal silicide" (40) comprises tungsten silicide. However, as pointed out above, Chung et al. do not teach an intermetallic compound which comprises a metal from each of layers 38 and 40 of Chung et al. Rather, Chung et al. teach that layer 36 is formed by the deposition of a titanium-tungsten or tungsten layer. Further, one would need to substitute tungsten for the disclosed aluminum or aluminum alloy in layer 40 of Chung. Such a need for selection negates anticipation.

Claims 32-34, and 42-49 are believed to be patentable for the same reasons discussed above with regard to the independent claims from which they depend.

Rejection under 35 U.S.C. 103(a) over Chung et al. U.S. Patent No. 4,910,578 in view of Okamoto U.S. Patent No. 4,910,578

Claim 36

Claim 36 recites that the composite structure has a thickness in the range of about 700 Angstroms to about 1800 Angstroms. The Examiner has acknowledged that Chung et al. do not disclose a composite structure having the claimed thickness range, but has reasoned that it would have been obvious to vary the thickness of Chung's composite structure to meet the claimed

thickness. Applicant disagrees. There is no motivation to modify the thickness of Chung's structure. Rather, the Examiner is using prohibited hindsight to reconstruct the reference to meet the claims. Even if the thickness were varied as suggested, the claimed composite structure would not result as Chung et al. do not teach or suggest a composite including an intermetallic compound which comprises metal from the first refractory metal silicide and a metal from the second refractory metal silicide.

Claim 38

Claim 38 is directed to a memory array comprising a plurality of memory cells, with each of the plurality of memory cells comprising at least one field effect transistor, and at least one local interconnect for connecting at least one of a source, drain, and gate of the field effect transistor in one of the plurality of memory cells to one of an active area within one memory cell or to one of a source, drain and date of a field effect transistor in another one of the plurality of memory cells. The local interconnect comprises a composite structure comprising a first refractory metal silicide, a second refractory metal silicide, and an intermetallic compound comprising a metal from the first refractory metal silicide and a metal from the second refractory metal silicide.

With regard to claim 38, the Examiner has taken the position that Chang et al. "discloses the claimed invention with the exception of teaching a memory array, and specifically disclosing what the local interconnect connects to." The Examiner asserts that Okamoto teaches an interconnect comprising a composite structure comprising a first metal silicide (4), a second metal silicide (8), and an intermetallic compound (10) comprising metal from the first metal silicide and metal from the second metal silicide, and that the interconnect structure can be used in memory arrays. Applicant disagrees.

Okamoto teaches a semiconductor device having a metal electrode interconnection film, a refractory metal silicide film, and a TiN barrier film between the refractory metal silicide film and the metal electrode interconnection film. In the method of Okamoto, a $TiSi_2$ film 4 reacts on an $MoSi_2$ film 8 to form a film 30 of $Ti_xMo_ySi_z$. A TiN film 10 is formed on the surface of film 8 to form a barrier layer. In making the rejection, the Examiner points out that Okamoto teaches that WSi_2 may be used in place of $MOSi_2$, and that TiW may be used in place of TiN film 10.

However, even if one were to make the proposed substitutions, Okamoto would not teach an intermetallic compound 10 which contains a metal from the first metal silicide 4 and the second metal silicide 8. Rather, Okamoto teaches that the barrier layer 10 is deposited by a sputtering method. The barrier layer 10 is clearly not formed from a reaction/etching of underlying layers as taught in the present invention. And, the differences in those processes result in compositional differences. Accordingly, even if combined, the teachings of Chung and Okamoto would not meet claim 38 as neither teaches a composite comprising an intermetallic layer comprising a metal from the first metal silicide and a metal from the second metal silicide.

Claims 46 and 47, which depend directly or indirectly from claim 38, are patentable for the same reasons that claim 38 is patentable.

Claims 39 and 40

For the same reasons discussed above with regard to claim 38, claims 39 and 40 are believed to be patentable over the combination of Chung and Okamoto.

Conclusion

The Board is requested to reverse the rejections of claims 31-49 in their entirety.

Respectfully submitted,

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CLAIMS APPENDIX

31. A local interconnect comprising:

a composite structure comprising a first metal silicide, a second metal silicide and an intermetallic compound reducing the resistance of said local interconnect, wherein said intermetallic compound comprises metal from said first metal silicide and metal from said second metal silicide, wherein said intermetallic compound contains no non-metallic materials.

32. The local interconnect of claim 31, wherein said first metal silicide and said second metal silicide each comprise at least one refractory metal.

33. The local interconnect of claim 32, wherein said at least one refractory metal for said first metal silicide and said second metal silicide is selected from the group consisting of chromium, cobalt, molybdenum, nickel, niobium, palladium, platinum, tantalum, titanium, tungsten, and vanadium.

34. The local interconnect of claim 32, wherein said first metal silicide comprises titanium silicide and said second metal silicide comprises tungsten silicide.

35. A local interconnect for connecting a first active semiconductor region to a second active semiconductor region on a substrate assembly, said first and second active semiconductor regions being separated by an insulating region, said local interconnect comprising:

a composite structure comprising a first refractory metal silicide, a second refractory metal silicide and an intermetallic compound reducing the resistance of said local interconnect, wherein said intermetallic compound comprises refractory metal from said first refractory metal silicide and refractory metal from said second refractory metal silicide, said refractory metal from said first refractory metal silicide being different from said refractory metal from said second refractory metal silicide, wherein said intermetallic compound contains no non-metallic materials.

36. The local interconnect of claim 35, wherein said composite structure has a thickness in the range of about 700 Angstroms to about 1800 Angstroms.

37. A semiconductor device comprising:

a substrate assembly having at least one semiconductor layer;

at least one field effect transistor formed in said at least one semiconductor layer, said least one field effect transistor having a source, a drain and a gate; and

a local interconnect for connecting at least one of said source, said drain and said gate to another active area within said substrate assembly, said local interconnect comprising a composite structure comprising a first refractory metal silicide, a second refractory metal silicide and an intermetallic compound reducing the resistance of said local interconnect, wherein said intermetallic compound comprises refractory metal from said first refractory metal silicide and refractory metal from said second refractory metal silicide, wherein said intermetallic compound contains no non-metallic materials.

38. A memory array comprising:

a plurality of memory cells arranged in rows and columns and formed on a substrate assembly having at least one semiconductor layer, each of said plurality of memory cells comprising at least one field effect transistor; and

at least one local interconnect for connecting at least one of a source, a drain and a gate of said at least one field effect transistor in one of said plurality of memory cells to one of an active area within said one memory cell or to one of a source, a drain and a gate of said at least one field effect transistor in another one of said plurality of memory cells, said local interconnect comprising a composite structure comprising a first refractory metal silicide, a second refractory metal silicide and an intermetallic compound reducing the resistance of said local interconnect, wherein said intermetallic compound comprises refractory metal from said first refractory metal silicide and refractory metal from said second refractory metal silicide, wherein said intermetallic compound contains no non-metallic materials.

39. The memory array of claim 38, further comprising a plurality of local interconnects for connecting additional active areas within each of said plurality of memory cells.

40. The memory array of claim 38, further comprising a plurality of local interconnects for connecting together active areas from different memory cells.

41. A local interconnect comprising:

a composite structure comprising a first metal silicide, a second metal silicide and an intermetallic compound formed by a reaction between said first metal silicide and said second metal silicide, wherein said intermetallic compound comprises metal from said first metal silicide and metal from said second metal silicide reducing the resistance of said local interconnect, wherein said intermetallic compound contains no non-metallic materials.

42. The local interconnect of claim 35, wherein said first metal silicide comprises titanium silicide and said second metal silicide comprises tungsten silicide.

43. The local interconnect of claim 41, wherein said intermetallic compound comprises titanium tungsten.

44. The semiconductor device of claim 37, wherein said first metal silicide comprises titanium silicide and said second metal silicide comprises tungsten silicide.

45. The semiconductor device of claim 44, wherein said intermetallic compound comprises titanium tungsten.

46. The memory array of claim 38, wherein said first metal silicide comprises titanium silicide and said second metal silicide comprises tungsten silicide.

47. The memory array of claim 46, wherein said intermetallic compound comprises titanium tungsten.

48. The local interconnect of claim 41, wherein said first metal silicide comprises titanium silicide and said second metal silicide comprises tungsten silicide.

49. The local interconnect of claim 48, wherein said intermetallic compound comprises titanium tungsten.

EVIDENCE APPENDIX

NONE

RELATED PROCEEDINGS APPENDIX

See attached Decision on Appeal

MIO 0024PA

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte JIGISH D. TRIVEDI

Appeal No. 2002-0043
Application No. 08/915,658

ON BRIEF

Before JERRY SMITH, GROSS, and BARRY, *Administrative Patent Judges.*
BARRY, *Administrative Patent Judge.*

DECISION ON APPEAL

A patent examiner rejected claims 31-40. The appellant appeals therefrom under 35 U.S.C. § 134(a). We affirm.

BACKGROUND

The appellant's invention is a local interconnect for an integrated circuit ("IC"). In the manufacture of ICs, interconnects provide electrical paths between field effect transistors and other devices fabricated on a semiconductor substrate and the external circuitry used to pass data to and from these devices. In particular, polycide structures are commonly used to form the gate of a metal oxide semiconductor field effect

transistor ("MOSFET"). A local interconnect is typically used to connect the polycide gate to active semiconductor areas, such as the source or drain of another MOSFET. A local interconnect may also be used to connect active semiconductor areas to other active semiconductor areas separated by an insulating region, such as a field oxide region.

Titanium silicide ($TiSi_2$) is commonly used as a local interconnect for connecting desired polycide gates and active semiconductor areas. (Spec. at 1.) While $TiSi_2$ is a low resistive conductor, the appellant asserts that the titanium theren is susceptible to oxidation during and after its formation. (*Id.* at 2.) The resultant titanium dioxide (TiO_2) increases the sheet resistance of the interconnect,[1] he adds, thereby increasing power dissipation and reducing the speed of the device. (*Id.*) Further, the TiO_2 impedes the formation of good electrical contacts on the $TiSi_2$ interconnect and poses adhesion problems when subsequent layers are deposited on top of the interconnect. (*Id.*)

The appellant's local interconnect is formed from a refractory metal silicide. (*Id.* at 1.) The metal silicide is patterned to form the boundaries of the local interconnect and then reacted with an underlying layer of metal. Silicon from the metal silicide

[1]Sheet resistance is an electrical quantity measured on a thin layer and has the units of ohms/square. (Spec. at 2.)

combines with the underlying metal to form another metal silicide. An intermetallic compound of titanium-tungsten (TiW), comprised of metal from the underlying metal layer and metal from the metal silicide, is also formed. The appellant asserts that the intermetallic TiW reduces the resistance of the local interconnect while also increasing its adhesion characteristics. (*Id.* at 13.)

A further understanding of the invention can be achieved by reading the following claim:

> 31. A local interconnect comprising:
>
> a composite structure comprising a first metal silicide, a second metal silicide and an intermetallic compound comprising metal from said first metal silicide and metal from said second metal silicide.

Claims 31-34 stand rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 4,910,578 ("Okamoto"). Claims 35-40 stand rejected under 35 U.S.C. § 103(a) as obvious over Okamoto in view of U.S. Patent No. 5,227,333 ("Shepard").

OPINION

At the outset, we recall that claims that are not argued separately stand or fall together. *In re Kaslow*, 707 F.2d 1366, 1376, 217 USPQ 1089, 1096 (Fed. Cir. 1983) (citing *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979)). Here, the appellant

argues claims 31-34 as a group, (Appeal Br. at 3), and claims 35-40 as another group. (*Id.*) Therefore, claims 32-34 stand or fall with representative claim 31, and claims 36-40 stand or fall with representative claim 35.

With this representation in mind, rather than reiterate the positions of the examiner or appellant *in-toto*, we address the three points of contention therebetween. First, the examiner asserts, "Okamoto teaches the conditions under which the composite film may be formed in Col. 5, lines 35-61, and that a ternary silicide film is indeed an intermetallic compound." (Examiner's Answer at 7.) The appellant argues, "[s]ummarizing, Okamoto explicitly teaches the formation of a ternary silicide, not an intermetallic compound." (Appeal Br. at 7.)

"Analysis begins with a key legal question -- *what* is the invention *claimed*?" *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1567, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987). In answering the question, "the Board must give claims their broadest reasonable construction. . . ." *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1668 (Fed. Cir. 2000). "Moreover, limitations are not to be read into the claims from the specification." *In re Van Geuns*, 988 F.2d 1181, 1184, 26 USPQ2d 1057, 1059 (Fed. Cir. 1993) (citing *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989)).

Here, representative claims 31 and 35 specify in pertinent part the following limitations: "an intermetallic compound. . . ." The adjective "intermetallic" means "composed of two or more metals or of a metal and a nonmetal. . . ." *Webster's Ninth New Collegiate Dictionary* 632 (1990)(copy attached). As noted by the appellant, "[a]ccording to Webster's, a compound of a metal and a non-metal is considered to be 'intermetallic.'" (Appeal Br. at 7.) Kirk-Othmer's Encyclopedia of Chemical Technology's reference to molybdenum silicide ($MoSi_2$) as an "intermetallic compound[]," vol. 20, p. 826 (1978)(copy attached), moreover, evidences that an intermetallic compound may include a nonmetal.

Giving the representative claims their broadest, reasonable construction, the limitations do not limit the components of "an intermetallic compound" to only metals as argued by the appellant. (Appeal Br. at 7; Reply Br. at 3.) Instead, claims 31 and 35 merely require a compound that includes a metal.

"[H]aving ascertained exactly what subject matter is being claimed, the next inquiry must be into whether such subject matter is novel." *In re Wilder*, 429 F2d 447, 450, 166 USPQ 545, 548 (CCPA 1970). "[A]nticipation is a question of fact." *Hyatt*, 211 F.3d at 1371, 54 USPQ2d at 1667 (citing *Bischoff v. Wethered*, 76 U.S. (9 Wall.) 812, 814-15 (1869); *In re Schreiber*, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431

(Fed. Cir. 1997)). "A claim is anticipated . . . if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros., Inc. v. Union Oil Co.*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) (citing *Structural Rubber Prods. Co. v. Park Rubber Co.*, 749 F.2d 707, 715, 223 USPQ 1264, 1270 (Fed. Cir. 1984); *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548, 220 USPQ 193, 198 (Fed. Cir. 1983); *Kalman v. Kimberly-Clark Corp.*, 713 F.2d760, 771, 218 USPQ 781, 789 (Fed. Cir. 1983)).

Here, we find that Okamoto teaches an intermetallic compound, viz., "a $Ti_xMo_ySi_z$ film 30," col. 5, l. 60, which is shown in Figure 4D of the reference. Because the $Ti_xMo_ySi_z$ film includes the metals titanium (Ti) and molybdenum (Mo), it is an "intermetallic compound."

Second, the examiner asserts, "Okamoto . . . shows in Fig. 4D an interconnect comprising a composite structure comprising a first metal silicide 4, a second metal silicide 8, and an intermetallic compound 30 comprising metal from the first metal silicide and metal from the second metal silicide." (Examiner's Answer at 3.) The appellant argues, "Okamoto does not mention expressly or inherently the formation of an intermetallic compound from two different metals in different metal silicide layers."

Claim 31 further specifies in pertinent part that its intermetallic compound "compris[es] metal from said first metal silicide and metal from said second metal silicide." Similarly, claim 35 further specifies in pertinent part its intermetallic compound "compris[es] refractory metal from said first refractory metal silicide and refractory metal from said second refractory metal silicide. . . ." Giving the representative claims their broadest, reasonable construction, the limitations merely require that the intermetallic compound comprise metal from two metal silicide layers.

We find that Okamoto's intermetallic compound comprises metal from two metal silicide layers. Specifically, the reference's $Ti_xMo_ySi_z$ film 30 comprises the metal Ti from the reference's "$TiSi_2$ film 4," col. 5, l. 37, and the metal Mo from its "$MoSi_2$ film 8. . ." *Id.* Therefore, we affirm the rejection of claim 31 and of claims 32-34, which fall therewith.

Third, the examiner asserts, "it would have been obvious to one of ordinary skill in the art to use the interconnect of Okamoto to connect a source, drain or gate to another area within a substrate assembly as taught by Shepard." (Examiner's Answer at 5.) The appellant argues, "the teachings of Okamoto would not be properly combinable because a completely different semiconductor device is taught using different materials." (Appeal Br. at 9.)

Claim 35 further specifies in pertinent part the following limitations: "[a] local interconnect for connecting a first active semiconductor region to a second active semiconductor region on a substrate assembly. . . ." Giving the claim its broadest, reasonable construction, the limitations merely require connecting active semiconductor regions on a substrate.

Obviousness follows *ipso facto* from an anticipatory reference. *RCA Corp. v. Applied Digital Data Sys., Inc.*, 730 F.2d 1440, 1446, 221 USPQ 385, 390 (Fed. Cir. 1984). "[A] disclosure that anticipates under Section 102 also renders the claim invalid under Section 103, for 'anticipation is the epitome of obviousness.'" *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548, 220 USPQ 193, 198 (Fed. Cir. 1983) (quoting *In re Fracalossi*, 681 F.2d 792, 794, 215 USPQ 569, 571 (CCPA 1982)).

Here, we find that Okamoto's "unreactive $TiSi_2$ film 4, . . . $Ti_xMo_ySi_z$ film 30 and an unreactive $MoSi_2$ film 8 as shown in FIG. 4D," col. 5, ll. 59-61, collectively connect two active semiconductor regions on a substrate. While Figure 4D specifically shows a "formation of ternary silicide films in the semiconductor device according to the embodiment of the present invention," col. 3, ll. 41-44, Figures 3A-3I more generally depict formation of the invention. "Referring to FIG. 3D, a impurity diffusion layer 5 is formed in a region of the silicon substrate 1 covered by the $TiSi_2$ film 4 through ion

implantation and heat treatment, so that the impurity diffusion layer 5 and the silicon substrate 1 form a P-N junction." Col. 4, ll. 4-8. "The silicon substrate 1 and the impurity diffusion layer are in P-N junction with each other to form a path for electric signals, which path corresponds to source/drain layers of a MOS element." Col. 1, ll. 36-39. This source layer and drain layer are the active semiconductor regions that the combination of Okamoto's $TiSi_2$ film 4, $Ti_xMo_ySi_z$ film 30, and $MoSi_2$ film 8 connects.

"[S]ince anticipation is the ultimate of obviousness, . . . the subject matter of these claims is necessarily obvious and we need not consider them further." *In re Baxter Travenol Lab.*, 952 F.2d 388, 392, 21 USQP2d 1281, 1285 (Fed. Cir. 1991) (citing *Fracalossi*, 681 F.2d at 794, 215 USPQ at 571. Nonetheless, regarding the combination of Okamoto and Shepard, "[w]hat appellant[] overlook[s] is that it is not necessary that the inventions of the references be physically combinable to render obvious the invention under review." *In re Sneed*, 710 F.2d 1544, 1550, 218 USPQ 385, 389 (Fed. Cir. 1983) (citing *Orthopedic Equip. Co. v. United States*, 702 F.2d 1005, 1013, 217 USPQ 193, 200 (Fed. Cir. 1983); *In re Andersen*, 391 F.2d 953, 958, 157 USPQ 277, 281 (CCPA 1968)). *See also In re Nievelt*, 482 F.2d 965, 968, 179 USPQ 224, 226 (CCPA 1972) ("Combining the teachings of references does not involve an ability to combine their specific structures."). The test for obviousness is not whether the features of a reference may be bodily incorporated into the structure of another

reference but what the combined teachings of those references would have suggested to one of ordinary skill in the art. *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981).

Here, combining the teachings of Okamoto and Shepard does not involve an ability to combine their specific structures. "A process for making a local interconnection of devices on a semiconductor substrate is disclosed [by Shepard]." Abs. ll. 1-2. It is for this general teaching of interconnecting devices on a substrate, rather than the specific structure of the interconnection, that the examiner relies on Shepard. The appellant's argument overlooks "the relevant combined teachings of the references." *Andersen*, 391 F.2d at 958, 157 USPQ at 281 (dismissing the argument that a combination would result in an inoperative structure). Therefore, we affirm the rejection of claim 35 and of claims 36-40, which fall therewith.

CONCLUSION

In summary, the rejection of claims 31-34 under § 102(b) and the rejection of claims 35-40 under § 103(a) are affirmed. Our affirmance is based only on the arguments made in the briefs. Arguments not made therein are neither before us nor at issue but are considered waived. No time for taking any action connected with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

JERRY SMITH
Administrative Patent Judge

ANITA PELLMAN GROSS
Administrative Patent Judge

LANCE LEONARD BARRY
Administrative Patent Judge

) BOARD OF PATENT
) APPEALS
) AND
) INTERFERENCES

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¹in·ter·me·di·ate \ˌint-ər-'mēd-ē-ət\ *adj* [ML *intermediatus*, fr. L *intermedius*, fr. *inter-* + *medius* mid, middle — more at MID] (15c) 1 : being or occurring at the middle place, stage, or degree or between extremes 2 : of or relating to an intermediate school ⟨an ~ curriculum⟩ — **in·ter·me·di·ate·ly** *adv* — **in·ter·me·di·ate·ness** *n*

²intermediate *n* (1650) 1 : one that is intermediate 2 : MEDIATOR, GO-BETWEEN 3 : a chemical compound formed as an intermediate step between the starting material and the final product 4 : an automobile larger than a compact but smaller than a full-sized automobile

³in·ter·me·di·ate \-ē-ˌāt\ *vi* [ML *intermediatus*, pp. of *intermediare*, fr. L *inter-* + LL *mediare* to mediate] (1610) 1 : INTERVENE, INTERPOSE 2 : to act as an intermediate

intermediate host *n* (1878) 1 : a host which is normally used by a parasite in the course of its life cycle and in which it may multiply asexually but not sexually 2 a : RESERVOIR 3 b : VECTOR

intermediate school *n* (1842) 1 : JUNIOR HIGH SCHOOL 2 : a school usu. comprising grades 4 to 6

in·ter·me·di·a·tion \ˌint-ər-ˌmēd-ē-'ā-shən\ *n* (1602) : the act of coming between : INTERVENTION, MEDIATION

in·ter·me·din \ˌint-ər-'mēd-ᵊn\ *n* (1932) : MELANOCYTE-STIMULATING HORMONE

in·ter·ment \in-'tər-mənt\ *n* (14c) : the act or ceremony of interring

in·ter·me·tal·lic \ˌint-ər-mə-'tal-ik\ *adj* (1900) : composed of two or more metals or of a metal and a nonmetal; *esp* : being an alloy having a characteristic crystal structure and usu. a definite composition — **intermetallic** *n*

in·ter·mez·zo \ˌint-ər-'mets-(ˌ)ō, -'medz-\ *n, pl* **-zi** \-(ˌ)ē\ *or* **-zos** [It, deriv. of L *intermedius* intermediate] (1771) 1 : a short light entr'acte 2 a : a movement coming between the major sections of an extended musical work (as an opera) b : a short independent instrumental composition

in·ter·mi·na·ble \(')in-'tərm-(ə-)nə-bəl\ *adj* [ME, fr. LL *interminabilis*, fr. L *in-* + *terminare* to terminate] (15c) : having or seeming to have no end; *esp* : wearisomely protracted ⟨an ~ sermon⟩ — **in·ter·mi·na·ble·ness** *n* — **in·ter·mi·na·bly** \-blē\ *adv*

in·ter·min·gle \ˌint-ər-'miŋ-gəl\ *vb* (15c) : INTERMIX

in·ter·mis·sion \ˌint-ər-'mish-ən\ *n* [L *intermission-*, *intermissio*, fr. *intermissus*, pp. of *intermittere*] (15c) 1 : the act of intermitting : the state of being intermitted 2 : an interval between the parts of an entertainment (as the acts of a play) — **in·ter·mis·sion·less** *adj*

in·ter·mit \-'mit\ *vb* **-mit·ted; -mit·ting** [L *intermittere*, fr. *inter-* + *mittere* to send — more at SMITE] *vt* (1542) : to cause to cease for a time or at intervals : DISCONTINUE ~ *vi* : to be intermittent — **in·ter·mit·ter** *n*

in·ter·mit·tent \-'mit-ᵊnt\ *adj* [L *intermittent-*, *intermittens*, prp. of *intermittere*] (1603) : coming and going at intervals : not continuous ⟨~ rain⟩; *also* : OCCASIONAL ⟨~ trips abroad⟩ — **in·ter·mit·tence** \-ᵊn(t)s\ *n* — **in·ter·mit·tent·ly** *adv*

in·ter·mix \ˌint-ər-'miks\ *vb* [back-formation fr. obs. *intermixt* (intermingled), fr. L *intermixtus*, pp. of *intermiscēre* to intermix, fr. *inter-* + *miscēre* to mix — more at MIX] *vt* (1542) : to mix together ~ *vi* : to become mixed together — **in·ter·mix·ture** \-'miks-chər\ *n*

in·ter·mo·lec·u·lar \ˌint-ər-mə-'lek-yə-lər\ *adj* (1843) : existing or acting between molecules — **in·ter·mo·lec·u·lar·ly** *adv*

in·ter·mon·tane \ˌint-ər-'män-ˌtān\ *or* **in·ter·mont** \'int-ər-ˌmänt\ *adj* (1807) : situated between mountains ⟨an ~ basin⟩

¹in·tern *or* **in·terne** \in-'tərn, 'in-ˌ\ *adj* [MF *interne*, fr. L *internus*] *archaic* (1508) : INTERNAL

²in·tern \'in-ˌtərn, in-'\ *vt* (1866) : to confine or impound esp. during a war ⟨~ enemy aliens⟩ — **in·tern·ee** \(ˌ)in-ˌtər-'nē\ *n* — **in·tern·ment** \in-'tərn-mənt, 'in-ˌ\ *n*

³in·tern *also* **in·terne** \'in-ˌtərn\ *n* [F *interne*, fr. *interne*, adj.] (ca. 1879) : an advanced student or graduate usu. in a professional field (as medicine or teaching) gaining supervised practical experience (as in a hospital or classroom) — **in·tern·ship** \-ˌship\ *n*

⁴in·tern \'in-ˌtərn\ *vi* (ca. 1928) : to act as an intern

in·ter·nal \in-'tərn-ᵊl\ *adj* [L *internus*; akin to L *inter* between] (15c) 1 : existing or situated within the limits or surface of something: as a : situated within the body (2) : situated on the side (1) : situated near the inside of the body (2) : situated on the side toward the median plane of the body b : of, relating to, or occurring within the confines of an organized structure (as a club, company, or state) ⟨~ affairs⟩ ⟨a country's ~ food production⟩ 2 : relating or belonging to or existing within the mind 3 : INTRINSIC, INHERENT ⟨~ evidence of forgery in a document⟩ 4 : present or arising within an organism or one of its parts ⟨~ stimulus⟩ 5 : applied or intended for application through the stomach by being swallowed ⟨an ~ remedy⟩ — **in·ter·nal·i·ty** \ˌin-ˌtər-'nal-ət-ē\ *n* — **in·ter·nal·ly** \in-'tərn-ᵊl-ē\ *adv*

internal–combustion engine *n* (1884) : a heat engine in which the combustion that generates the heat takes place inside the engine proper instead of in a furnace

in·ter·nal·ise *Brit var of* INTERNALIZE

in·ter·nal·ize \in-'tərn-ᵊl-ˌīz\ *vt* **-ized; -iz·ing** (1884) : to give a subjective character to; *specif* : to incorporate (as values or patterns of culture) within the self as conscious or subconscious guiding principles through learning or socialization — **in·ter·nal·iza·tion** \-ˌtərn-ᵊl-ə-'zā-shən\ *n*

internal medicine *n* (ca. 1904) : a branch of medicine that deals with the diagnosis and treatment of nonsurgical diseases

internal respiration *n* (ca. 1890) : an exchange of gases between the cells of the body and the blood by way of the fluid bathing the cells — compare EXTERNAL RESPIRATION

internal rhyme *n* (1903) : rhyme between a word within a line and another either at the end of the same line or within another line

internal secretion *n* (1895) : HORMONE

¹in·ter·na·tion·al \ˌint-ər-'nash-nəl, -ən-ᵊl\ *adj* (1780) 1 : of, relating to, or affecting two or more nations ⟨~ trade⟩ 2 : of, relating to, or constituting a group or association having members in two or more nations ⟨~ movement⟩ 3 : active, known, or reaching beyond national boundaries ⟨the ~ set⟩ ⟨an ~ reputation⟩ — **in·ter·na·tion·al·i·ty** \-ˌnash-ə-'nal-ət-ē\ *n* — **in·ter·na·tion·al·ly** \-'nash-nə-lē, -ən-ᵊl-ē\ *adv*

²international *n* (1871) : one that is international; *esp* : an organization of international scope

international date line *n* (ca. 1909) : DATE LINE

in·ter·na·tion·al·ise *Brit var of* INTERNATIONALIZE

in·ter·na·tion·al·ism \-'nash-nəl-ˌiz-əm, -'nash-ən-ᵊl-\ *n* (1851) 1 : international character, principles, interests, or outlook 2 a : a policy of cooperation among nations b : an attitude or belief favo
policy — **in·ter·na·tion·al·ist** \-əst\ *n or adj*

in·ter·na·tion·al·ize \ˌint-ər-'nash-nəl-ˌiz, -'nash-ən-ᵊl-\ *vt* (ca.
make international; *also* : to place under international cont
posal to ~ the city⟩ — **in·ter·na·tion·al·iza·tion** \-ˌnash-nəl-
-ən-ᵊl-\ *n*

international law *n* (ca. 1828) : a body of rules that control o
rights of nations in their relations with each other

International Phonetic Alphabet *n* (1898) : IPA

international pitch *n* (1904) : a tuning standard of 440 vib
second for A above middle C

international relations *n pl but sing in constr* (1951) : a branc
cal science concerned with relations between nations and
with foreign policies

International Scientific Vocabulary *n* (ca. 1959) : a part of
lary of the sciences and other specialized studies that consis
or other linguistic forms current in two or more languages a
from New Latin in being adapted to the structure of the
languages in which they appear

International System *n* (1961) : METRIC SYSTEM

international unit *n* (1922) : a quantity of a biologic (as a vi
produces a particular biological effect agreed upon as an i
standard

international volt *n* (ca. 1926) : ²VOLT 2

in·ter·ne·cine \'int-ər-'nes-ˌēn, -'nēs-ᵊn, -'nē-ˌsīn, -nə-'sēn; in-
adj [L *internecinus*, fr. *internecare* to destroy, kill, fr. *inter-*
kill, fr. *nec-*, *nex* violent death — more at NOXIOUS] (1663)
by slaughter : DEADLY; *esp* : mutually destructive 2 : of,
or involving conflict within a group ⟨bitter ~ feuds⟩

in·ter·neu·ron \ˌint-ər-'n(y)ü-ˌrän, -'n(y)ù(ə)r-ˌän\ *n* (ca. 193
nuncial neuron — **in·ter·neu·ro·nal** \-'n(y)ùr-ən-ᵊl, -nyù-'rō

in·ter·nist \'in-ˌtər-nəst\ *n* (1904) : a specialist in internal m
as distinguished from a surgeon

in·ter·node \'int-ər-ˌnōd\ *n* [L *internodium*, fr. *inter-* +
(1667) : an interval or part between two nodes (as of a ste
nod·al \ˌint-ər-'nōd-ᵊl\ *adj*

in·ter·nu·cle·ar \ˌint-ər-'n(y)ü-klē-ər, ÷-kyə-lər\ *adj* (1878)
occurring between atomic or biological nuclei

in·ter·nun·ci·al \ˌint-ər-'nən(t)-sē-əl, -'nün(t)-\ *adj* (1845)
lating to an internuncio 2 : serving to link sensory and m

in·ter·nun·cio \ˌint-ər-'nən(t)-sē-ˌō, -'nün(t)-\ *n* [It *internun*
ternuntius, *internuncius*, fr. *inter-* + *nuntius*, *nuncius* mess
1 : a messenger between two parties : GO-BETWEEN 2 : a
of lower rank than a nuncio

in·tero·cep·tive \ˌint-ə-rō-'sep-tiv\ *adj* [*inter-* (as in *inter*
-ceptive (as in *receptive*)] (1906) : of, relating to, or being
within the body and esp. in the viscera

in·tero·cep·tor \-tər\ *n* (1906) : a sensory receptor excited
tive stimuli

in·ter·pel·late \ˌint-ər-'pel-ˌāt, -pə-'lāt\ *vt* **-lat·ed; -lat·ing** [L
pp. of *interpellare* to interrupt, fr. *inter-* + *-pellare* (fr. *p*
— more at FELT] (1874) : to question (as a foreign min
concerning an official action or policy or personal conc
pel·la·tion \-pə-'lā-shən\ *n* — **in·ter·pel·la·tor** \-'pel-ˌāt-ər

in·ter·pen·e·trate \ˌint-ər-'pen-ə-ˌtrāt\ *vt* (1809) : to pene
~ *vi* : to penetrate between, within, or throughout : PE
ter·pen·e·tra·tion \-ˌpen-ə-'trā-shən\ *n*

in·ter·per·son·al \-'pərs-nəl, -ᵊn-əl\ *adj* (1842) : being,
involving relations between persons — **in·ter·per·son·al·i·**

in·ter·phase \'int-ər-ˌfāz\ *n* (1925) : the interval between
mitotic or meiotic division and the beginning of another

in·ter·plant \ˌint-ər-'plant\ *vt* (1911) : to plant a crop bet
another kind); *also* : to set out young trees among (exist

in·ter·play \'int-ər-ˌplā\ *n* (1862) : INTERACTION (the
forces⟩ — **in·ter·play** \ˌint-ər-'\ *vi*

in·ter·plead \ˌint-ər-'plēd\ *vi* [AF *enterpleder*, fr. *enter-* in
plead, fr. OF *plaidier* — more at PLEAD] (1567) : to
each other in order to determine a right on which the
party depends

¹in·ter·plead·er \-ər\ *n* [AF *enterpleder*, fr. *enterpleder*
proceeding to enable a person to compel parties makin
against him to litigate the matter between themselves

²interpleader *n* (ca. 1846) : one that interpleads

in·ter·po·late \in-'tər-pə-ˌlāt\ *vb* **-lat·ed; -lat·ing** [L *in*
interpolare to refurbish, alter, interpolate, fr. *inter-* +
to polish)] *vt* (1612) 1 a : to alter or corrupt (as a t
new or foreign matter b : to insert (words) into a te
versation 2 : to insert between other things or parts
: to estimate values of (a function) between two kn
: to make insertions (as of estimated values) *syn* see
ter·po·la·tion \-ˌtər-pə-'lā-shən\ *n* — **in·ter·po·la·tive**
adj — **in·ter·po·la·tor** \-ˌlāt-ər\ *n*

in·ter·pose \ˌint-ər-'pōz\ *vb* **-posed; -pos·ing** [MF *inter*
ponere (perf. indic. *interposui*), fr. *inter-* + *ponere* t
POSITION] *vt* (1599) 1 a : to place in an intervenin
put (oneself) between : INTRUDE 2 : to put forth by w
or intervention 3 : to introduce or throw in betwe
conversation or argument ~ *vi* 1 : to be or come
step in between parties at variance : INTERVENE 3 :
ter·pos·er *n*

syn INTERPOSE, INTERFERE, INTERVENE, MEDIATE: IN
come or go between. INTERPOSE implies no more th
implies a getting in the way or otherwise hinderin
imply an occurring in space or time between two t
in to halt or settle a quarrel or conflict; MEDIATE
between hostile factions; INTERCEDE implies actin
offender in begging mercy or forgiveness. *syn* see
DUCE

in·ter·po·si·tion \-pə-'zish-ən\ *n* (14c) 1 a : the ac
: the action of a state whereby its sovereignty is
citizens and the federal government 2 : something

in·ter·pret \in-'tər-prət, -ˌpret\ *vb* [ME *interpreten*, fr.
preter, fr. L *interpretari*, fr. *interpret-*, *interpres* ager
preter] *vt* (14c) 1 : to explain or tell the meaning

AFA 3PW

PTO/SB/17 (12-04)
Approved for use through 07/31/2006. OMB 0651-0032
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Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	08/915,658
Filing Date	August 21, 1997
First Named Inventor	Jigish D. Trivedi
Examiner Name	Ginette Peralta
Art Unit	2814
Attorney Docket No.	MIO 0024 PA/40509.49

METHOD OF PAYMENT (check all that apply)

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES Fee ($)	FILING FEES Small Entity Fee ($)	SEARCH FEES Fee ($)	SEARCH FEES Small Entity Fee ($)	EXAMINATION FEES Fee ($)	EXAMINATION FEES Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	_____	x _____	= _____

HP = highest number of total claims paid for, if greater than 20

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	_____	x _____	= _____

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims Fee ($)	Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____ / 50 =	_____ (round up to a whole number) x	_____	= _____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other: Payment for Brief on Appeal	500.00

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 29,001	Telephone (937) 449-6400
Name (Print/Type)	Timothy W. Hagan		Date September 1, 2005